

CS 64

SYED AMMAL ENGINEERING COLLEGE

B.E / B.Tech Degree Examination – Periodical Test-I

COMMON TO III CSE A & B

10144CS604-ADVANCED COMPUTER ARCHITECTURE

Date: 08.02.2013

Time: 2 Periods

Maximum: 50 Marks

Answer All Questions

PART- A (5 x 2 = 10)

- 1.What are the limits on ILP?
- 2.How can a deferred exception be resolved?
- 3.What is multiprocessor cache coherence?
- 4.Distinguish between shared memory and message passing multiprocessor.
- 5.What is loop carried dependence and dependence distance?

PART-B (2 ½ *16=40)

- 6.(a).Compare Hardware and Software speculation mechanisms. (8)
(or)
(b).Describe the architectural features of EPIC processor in detail. (8)
- 7.(a).Explain in detail how compiler support can be used to increase the amount of parallelism that can be exploited in a program. (16)
(or)
(b).(i)With examples, explain how do you detect and enhance Loop-Level Parallelism? (8)
(ii) Explain the architecture of a typical VLIW processor in detail. (8)
- 8.(a).Describe the basic structure of a symmetric-shared memory architecture in detail. (16)
(or)
(b).Explain Intel IA-64 Architecture in detail with suitable reference to Itanium processor (16)